ABSTRACT OF THE DISCLOSURE

A first drive voltage generating section corresponds to a first motor, and a second drive voltage generating section corresponds to a second motor. Each of the first drive voltage generating section and the second drive voltage generating section includes switching elements, an A/D converter, and an MPU. Each A/D converter samples an analog signal representing a load state of the corresponding motor. A clock circuit synchronizes the control periods of the drive voltage generating sections. Each MPU commands the corresponding A/D converter to sample the analog signal at timing where no switching is performed by any of the switching elements in the drive voltage generating sections. Therefore, the analog signals representing the load states of the motors are preferably sampled without being influenced by noise generated by switching.